# **Department of Computer Science and Engineering**

### **BRAC University**

### **CSE 260: Digital Logic Design**

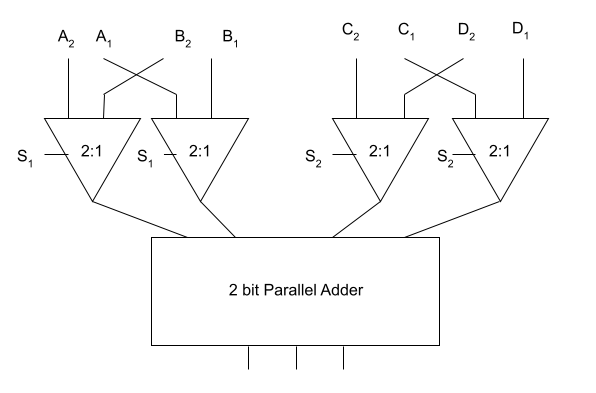
# **Experiment # 8**

***Design and Implementation of the following circuit:***

Four 2 bit numbers A, B, C, D and two selection variables S1 and S2 are available. S1 will select either A or B and S2 will select either C or D. Depending on the two selection variables, the circuit will work in the following way.

| **S1** | **S2** | **Operation** |
| --- | --- | --- |
| 0 | 0 | A+C |
| 0 | 1 | A+D |
| 1 | 0 | B+C |
| 1 | 1 | B+D |

**IC: MUX (74153) Adder: 7483**

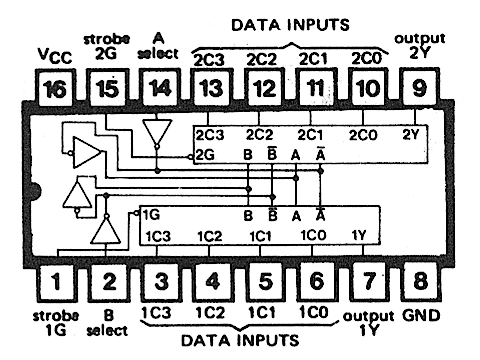
**Report:**

The report should cover the followings

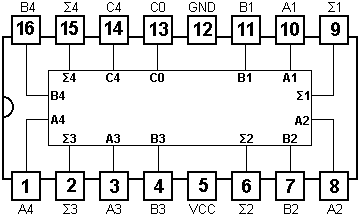
1. Name of the experiment
2. Objective
3. Required Components and Equipments
4. Experimental Setup (i.e., diagram of the circuit)
5. Results and Discussions

Draw a circuit diagram which will compare three 4 bit numbers. You have Magnitude Comparators and 2:1 MUXs.

**Mux 74153**



**Adder 7483**

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Set: C4 = COUT, C0 =0

***Strobe = Low***

**MUX Connection:**

**Make 4:2 Mux to 2:1 Mux in the following way**

Short Selector A and B

Selector Data Input (Active) Output (1Y) Output (2Y)

00 1C0, 2C0 1C0 2C0

11 1C3, 2C3 1C3 2C3

Give Inputs:

First IC Connection: A = B= S1 (Selector)

1C0 → A1

1C3→ B1

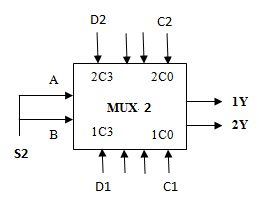
2C0→ A2

2C3→ B2







Second IC Connection: C = D = S2 (Selector)

1C0 → C1

1C3→ D1

2C0→ C2

2C3→ D2

| Selector: S1  (First MUX) | OUTPUT of MUX-1 | | Selector: S2  (Second MUX) | OUTPUT of MUX-2  **1Y 2Y** | |
| --- | --- | --- | --- | --- | --- |
| **1Y** | **2Y** |
| 0 | A1 | A2 | 0 | C1 | C2 |
| 0 | A1 | A2 | 1 | D1 | D2 |
| 1 | B1 | B2 | 0 | C1 | C2 |
| 1 | B1 | B2 | 1 | D1 | D2 |